

FIG. 4

The diagram illustrates a digital filter circuit 105. It features two main inputs: I'_1 OR Q'_1 and F_{SAMPLE} . The I'_1 OR Q'_1 input is connected to a multiplexer 72, which selects between a feedback signal $X(n-1)$ from a REGISTER and a new input $X(n)$ from a multiplexer 80. The F_{SAMPLE} input is connected to a multiplexer 84, which selects between a feedback signal $Y(n)$ from a multiplexer 92 and a new input $Y(n)$ from a multiplexer 90. The circuit contains two adders (82 and 90), a multiplier (86), and a delay element (74). The output of the circuit is I_2 OR Q_2 .

